Monolithic Circuit for Reflection Coefficient Measurement

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Abstract—**A monolithic circuit for measuring complex reflection coefficient using fixed-probe voltage sampling has been investigated. Ion implanted GaAs Schottky diodes, with built-in isolation resistance, have been used as voltage samplers along a microstrip transmission line on semi-insulating GaAs. An algorithm for determining reflection coefficient from three detected dc voltages is described. Circuit analysis and modeling, dc voltage calculations, and experimental results are presented for the 5 to 18 GHz frequency range.**

I. Introduction

In microwave and millimeter-wave monolithic circuits, it is normal to have many functional circuits interconnected so that access to inner stages for testing them is not possible. A small circuit integrated into more complex circuits at critical points can provide valuable interstage test information. Such a test circuit must be small so that it does not use much expensive real estate, and it must be simple so that it is much less likely to fail than the circuitry it is testing. The monolithic circuit to be described here provides simplicity and small size.

II. Monolithic Circuit Design

The general concept of fixed-probe voltage sampling along a transmission line to measure load impedance is described in [1], wherein the work of Taylor [2] is also summarized. It is also reviewed in [3] and [4]. The purpose of the work here is to find an embodiment of it for monolithic microwave and millimeter-wave circuit testing. Two ratios of dc-detected voltages along a transmission line are needed to determine a complex load impedance—three diodes can provide these two ratios. The experimental circuits are shown schematically in Fig. 1. Five test circuits were used and Fig. 2 is a photograph of them. The five circuits differ only in their nominal load: Short circuit, 25 ohms, 50 ohms, 100 ohms, and open circuit, left to right in the photograph. Since the open circuit load could not provide a dc return for the diode bias, the return is provided as shown in Fig. 1 for all of the circuits, and a dc-blocking capacitor of 7.56 pF is included in the load. A bias current of approximately 10 μA, giving maximum detector sensitivity, was used. The detected output voltage was taken across the 100-kΩ bias resistor in Fig. 1. Attaching similarly to $D1$ and $D2$ gives three detected dc voltages at three known positions along uniform 50Ω microstrip transmission line. From this information the load impedance can be calculated as will be discussed later. Adams-Russell Semiconductor Center fabricated the circuits. The substrate material is semi-insulating GaAs 95 μm thick, with the diodes selectively ion-implanted. The main microstrip transmission line is 71 μm wide giving 50Ω characteristic impedance.

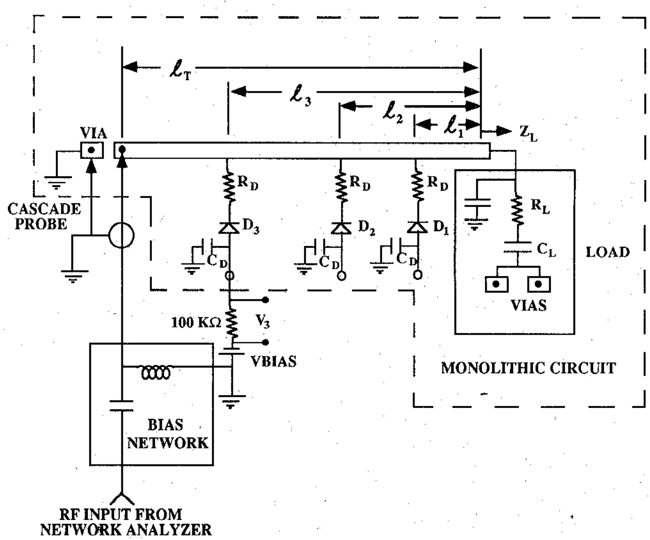

Fig. 1. Simplified schematic representation of experimental circuit.

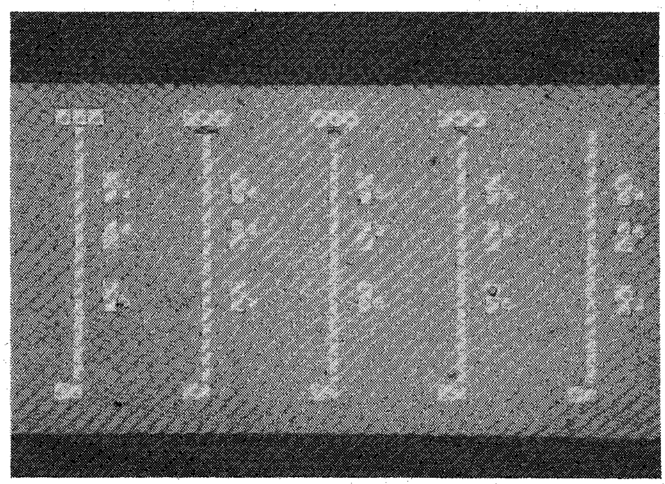

Fig. 2. Photograph of experimental circuits.

To provide RF isolation of the diodes from the 50Ω transmission line, a large series resistance was included in the diode design. The diode's Schottky finger is 5 μm long and 2 μm wide but there is no wrap-around cathode encir-

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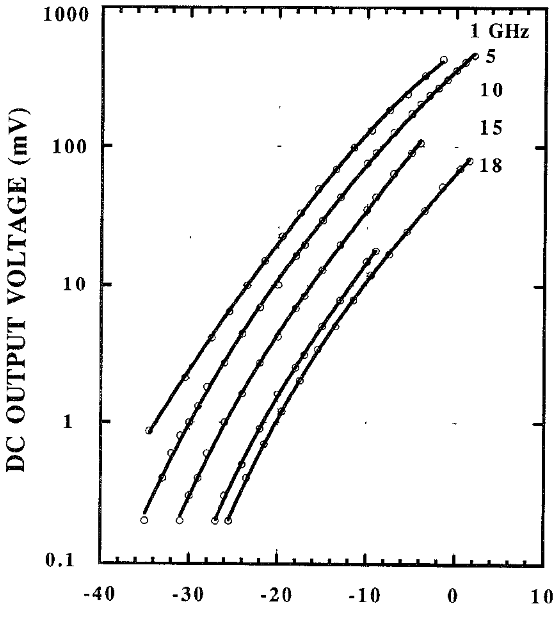

Fig. 3. Detector diode RF performance.

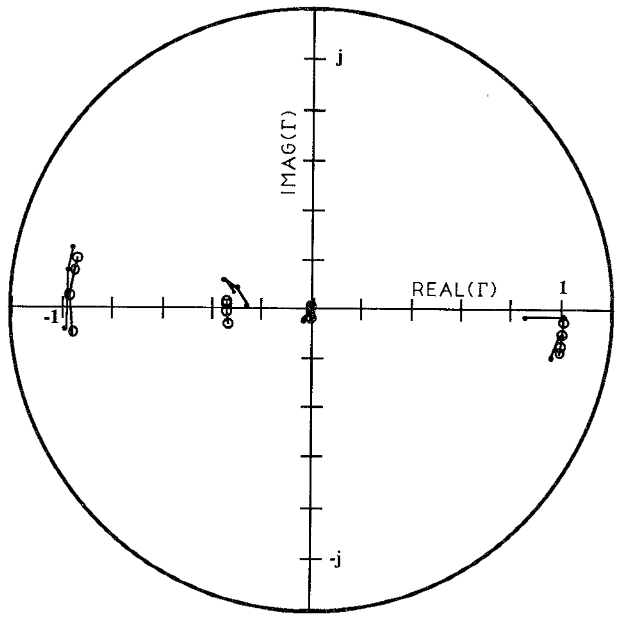

Fig. 4. Measured reflection coefficient of nominal loads: short circuit, 25 ohms, 50 ohms, and open circuit. Circles—derived from network analyzer measurements; dots—derived from dc voltage sampling. Frequencies plotted are 5, 10, 15, and 18 GHz, increasing in the clockwise direction.

cling the finger, as is usually used for minimizing the series resistance. The region under and around the finger, including a 3 μm gap between the end of the finger and the main 50 Ω transmission line, was ion implanted to about $1.5 \times 10^{17}/\text{cm}^3$ uniform n-type doping, about 0.2 μm thick. This creates a good Schottky finger contact but with a large series resistance of about 750 ohms.

RF performance of the detectors is shown in Fig. 3. These curves give the detected dc voltage across a 100-kΩ load resistance versus the RF power feeding the circuit from the Cascade probe as shown in Fig. 1. For these measurements the load was an open circuit and the diode was the one closest to the load. The curves show nearly square law behavior from less than 1 mV dc to several tens of millivolts. Square law operation was assumed in the theoretical analysis which will follow.

Selective ion implantation was also used for the transmission line load resistors. Nitride dielectric was used as the insulating film for the 7.56 pF blocking capacitor, CL, and for the 6.3 pF diode output bypass capacitor, CD.

III. Theory

To calculate the RF voltage along a transmission line, the load impedance and the line characteristics must be accurately known. A model of the transmission line circuit and load element was developed for each of the five circuits to derive the load impedance from network analyzer measurements. The lengths used in the experimental circuits for l_1, l_2, l_3, and l_T are 498, 809, 1430, and 2082 μm, respectively.

The total RF voltage at any point on a transmission line can be given by:

$$\text{VRF}(P) = [1 + \Gamma(P)]\text{VINC}(P), \quad (1)$$

where VINC(P) is the incident voltage and $\Gamma(P)$ is the reflection coefficient at that point; and the diode-rectified dc voltage output, assuming square law operation is:

$$\text{VDC}(P) = K\,|\text{VRF}(P)|^2, \quad (2)$$

where K is a rectification proportionality constant. Thus, the relative diode-detected dc voltages can be calculated from the "known" load information derived from the network analyzer measurements and from the transmission line parameters.

An algorithm was developed that uses the three measured detected voltages to find the load impedance. It uses the real and imaginary parts of the load reflection coefficient as search variables, recognizing their smooth, continuous behavior from -1 to $+1$ over the full range of possible load impedance values. Numerical problems that might arise from infinite impedances are thereby avoided. An initial search is done over the full range of values of these two variables (that is, over the full Smith chart) in increments small enough to find the vicinity of the global minimum of the error function. The error function used is the least-square error between the measured and calculated dc detected voltage ratios, VDC(3)/VDC(2) and VDC(3)/VDC(1). Subsequent search iterations are taken over successively smaller grids. This algorithm requires no initial estimate of the load impedance and always converges.

IV. Experiment

Fig. 4 shows the major results of the experimental circuit measurements. Agreement between HP 8510 network analyzer measurements (circles) and dc voltage measurements (dots) is reasonably good from 5 to 18 GHz. (The 100 ohm circuit had one bad diode, so no data is presented for it.) Though not shown on Fig. 4, the multiprobe method gave inaccurate results at 1 GHz, where the spacing between the two closest diodes is only 0.003 wavelengths. This is too short a distance to discern accurately the load dependent voltage variations along the line. The data at 5 GHz is satisfactory, however, so that a minimum length between the two closest diodes of about 0.02 wavelengths might be a good design guideline. The maximum operating frequency is above 18 GHz, but no measurements were made to characterize higher frequency performance. A practical upper frequency limit for the circuit described here exists because of the drop-off of diode sensitivity as Fig. 3 shows. For higher frequency operation different detector designs would be desirable, with reduced resistive isolation and with circuitry to improve diode matching.

V. Conclusion

The feasibility of a small and simple monolithic circuit on GaAs to measure complex impedance has been shown. The algorithm used to obtain the load reflection coefficient from three detected dc voltages was described. Good measurement results were obtained with experimental circuits in the 5 to 18 GHz range.

Acknowledgment

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